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Bound Techniques For VLSI (MIT/LCS/TR) By Frank
Thomson Leighton**

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Complexity Issues in VLSI. In particular, it describes optimal layouts for the shuffle-exchange graph, one of the best known networks for parallel computation.

L22 spreading metrics for vertex ordering problems

Frank Thomson Leighton, optimal layouts for the shuffle-exchange graph and other networks, MIT Press "Area-efficient graph layouts (for VLSI)," in

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@article{DHol92, author = "Erik H. D'Hollander", title = "Partitioning and Labeling of Loops by Unimodular Transformations", journal = "IEEE Trans. Parallel and

A layout for the shuffle- exchange network -

Abstract: This paper describes a technique for producing a VLSI layout of the shuffle-exchange graph. It is based on the layout procedure which lays out a graph by

Propositional dynamic logic of looping and

MIT LCS Technical Memo TM-116, Frank Thomson Leighton, we present several new layouts for the shuffle-exchange graph,

Permutation- exchange graphs that emulate the

Permutation-exchange graphs that emulate the binary cube Kleitman, D., Leighton, F. T., Lepley, M., and Miller, G. L., New layouts for the shuffle-exchange graph.

An area-efficient topology for vlsi implementation

found that the optimal shuffle-exchange (SE) graph layout from [9] applied to the implementation of Viterbi decoders

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An asymptotically optimal layout for the shuffle

The shuffle exchange graph is one of the best structures known for parallel An Asymptotically Optimal Layout for the Shuffle-Exchange Graph DANIEL

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LAYOUTSFORTHE SHUFFLE-EXCHANGE GRAPH 203 Miller who have described optimal layouts for small shuffle-exchange graphs in [LM81]. Subsequentto

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3. The Shuffle-Exchange Graph The shuffle-exchange graph on n vertices is defined only when n is a power of two. Each of the $n/2^k$ vertices can be identified with an

Upper bound for queue number of shuffle- exchange

UPPER BOUND FOR QUEUE NUMBER In this paper we prove that Shuffle-Exchange graph has a 3-queue layout, Suppose we have a linear graph layout

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node shuffle-exchange graph so that processor 000 initially has As an example. we have included a grid layout for tile 8-nodc shuffle-exchange graph in Figure 1

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